UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/931,104	08/17/2001	Eiji Yoshida	212881US2	3616

22850 7590 10/21/2003

OBLON, SPIVAK, MCCLELLAND, MAIER & NEUSTADT, P.C.
1940 DUKE STREET
ALEXANDRIA, VA 22314

EXAMINER	
MONDT, JOHANNES P	

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 10/21/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/931,104	YOSHIDA, EIJI	
	Examiner	Art Unit	
	Johannes P Mondt	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 June 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,4 and 6-20* is/are pending in the application.

4a) Of the above claim(s) *4,8-10 and 12-20* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,6 and 7* is/are rejected.

7)☒ Claim(s) *11* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☒ The proposed drawing correction filed on *18 June 2003* is: a)☒ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a)☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1)☒ Notice of References Cited (PTO-892)
2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3)☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4)☐ Interview Summary (PTO-413) Paper No(s). _____ .
5)☐ Notice of Informal Patent Application (PTO-152)
6)☐ Other:

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 06/18/03 has been entered.

Response to Arguments

2. Applicant's arguments, see Remarks in Request for Continued Examination, filed 6/18/3, with respect to the rejection of claims 1, 6-7 and 11 have been fully considered and are persuasive, because Petrosino does not teach that the gate of the first MOS transistor is insulated from the gate of the second MOS transistor. Therefore, the rejection based on Petrosino has been withdrawn. However, upon further consideration and search, new grounds of rejection have been discovered through Keown et al (5,286,656), who teach that for testing purposes a CMOS is connected in such a manner that said gates are in contact with respective test voltage outlets that are used respectively. Accordingly, new rejections for claims 1, 6 and 7 are presented. Although with the present rejection of claim 1 rejoinder of any previously non-elected claims cannot be allowed in any case, the examiner further reminds Applicant that a recitation of the intended use of the claimed invention must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the

claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim. In a claim drawn to a process of making, the intended use must result in a manipulative difference as compared to the prior art. See *In re Casey*, 152 USPQ 235 (CCPA 1967) and *In re Otto*, 136 USPQ 458, 459 (CCPA 1963).

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. ***Claim 1 and 6-7*** are rejected under 35 U.S.C. 102(b) as being anticipated by Keown et al (5,286,656). Keown et al teach (cf. Figure 2) a semiconductor device comprising:

a) a second MOS transistor (either TPMOS or TNMOS depending on whether the substrate of wafer is N-type or P-type), including a portion (S of TNMOS in case second MOS transistor is TNMOS; D of TPMOS in case second MOS transistor is TPMOS) that *can* be measured by a fluctuation in a potential;

b) a wire having a first end and second end (wire connecting S of TNMOS and D of TPMOS), the second end being connected with said portion that can be measured; and

c) an observation part including a pn junction *that can be* irradiated with a laser beam to detect said fluctuation in potential, wherein:

1) said observation part includes a first MOS transistor (the other of the TPMOS and TNMOS transistors that is NOT said second MOS transistor) having:

i) a source/drain region (D of TPMOS if TPMOS is said first transistor, and S of TNMOS if TNMOS is said first MOS transistor) including a first impurity region of first conductivity type (P-type for TPMOS, N-type for TNMOS), that is connected to said first end of said wire and that is formed within a second impurity region of second impurity type (N-type for TPMOS as first MOS transistor, P-type for TNMOS as first MOS transistor); and

ii) a gate electrode that is electrically insulated from a gate electrode of said second MOS transistor (please note that the gate of the TNMOS transistor is connected to a test voltage outlet DBP1 while the gate of the TPMOS transistor is connected to another test voltage outlet DBP2, while "respective test voltages are applied at test bond pads DBP1 and DBP2: hence these test voltages are independent and consequently DBP1 and DBP2, and hence the gates of the TNMOS and TPMOS transistors, are not electrically connected).

Although not specifically spelled out in Keown et al the existence of a substrate of a specific conductivity type and a well around either the TNMOS or TPMOS of opposite conductivity type depending on whether said substrate conductivity type is N-type or P-type is *inherent* in the CMOS device of Keown et al (cf. col. 4, lines 46-59) tested according to the description (cf. column 4, line 60 –column 6, line 43 and Figure 2) in Keown et al.

Although Keown et al do not teach ad a) that said portion *is* measured by fluctuation in potential, nor ad c) that said observation part *is* irradiated with a laser beam to detect said fluctuation in potential only the actual structure and not the use of the device is relevant to the presently elected invention (see Papers 4 and 6). Applicant is reminded that a recitation of the intended use of the claimed invention must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim. In a claim drawn to a process of making, the intended use must result in a manipulative difference as compared to the prior art. See *In re Casey*, 152 USPQ 235 (CCPA 1967) and *In re Otto*, 136 USPQ 458, 459 (CCPA 1963). In conclusion, Keown et al anticipate claim 1.

On claim 6: because current and voltage measurements are carried out and the current is known to be a function of gate characteristics (cf. column 5, lines 11-45) Keown et al actually carries out testing of the gates.

On claim 7: the said portion that can be measured is indeed either the source of TNMOS or the drain of TPMOS (see above, the discussion of claim 1).

Allowable Subject Matter

5. ***Claim 11*** is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. The following is a statement of reasons for the

indication of allowable subject matter: Keown et al do not teach that said first MOS transistor to include a third impurity region connected to said wire.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Johannes P Mondt whose telephone number is 703-306-0531. The examiner can normally be reached on 8:00 - 18:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J Flynn can be reached on 703-308-6601. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

JPM
October 19, 2003

NATHAN J. FLYNN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800